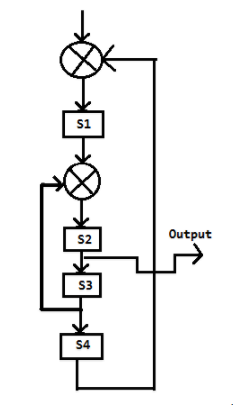
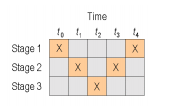
1A. Consider the following pipelined processor with four stages. This pipeline has a total evaluation time of six clock cycles. All successor stages must be used after each clock cycle.



1. Specify the reservation table for this pipeline with six columns and four rows.
2. List the set of forbidden latencies between task initiations.
3. Draw the state diagram which shows all possible latency cycles.
4. List all greedy cycles from state diagram.
5. What is value of MAL?

1B. Explain the different data hazards in a pipeline computer with an example for reach.

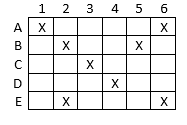
2A. Consider the following pipeline reservation table.



1. What are the forbidden latencies?
2. Draw the state transition diagram?
3. List all simple cycles and greedy cycles.
4. Compute MAL.
5. If clock rate is 20MHz find maximal throughput.

2B. Draw the data flow diagram for the interrupt cycle and explain the data transfer operations of that cycle.

3A. Consider the following pipeline reservation table. Find latency cycles, simple cycles and greedy cycles. Find out the MAL for this. If clock rate is 20MHz find maximal throughput.



3B. Briefly, explain Flynn’s MIMD architectural classification with a neat figure.

4A. Given the following Collision Vector, find latency cycles, simple cycles, greedy cycles and MAL.

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4B. Draw the functional structure of an array processor and briefly explain its operation.